

09/285,879

L Number	Hits	Search Text	DB	Time stamp
1	42686	power same table	USPAT; US-PGPUB	2001/11/04 15:33
4	117941	data with type	USPAT; US-PGPUB	2001/11/04 15:34
7	331	(power same table) same (data with type)	USPAT; US-PGPUB	2001/11/04 15:34
10	198248	driver	USPAT; US-PGPUB	2001/11/04 15:34
13	23	driver same ((power same table) same (data with type))	USPAT; US-PGPUB	2001/11/04 15:49
16	115703	power with (save or saving or conserve or conserving or conservation or reduce or reducing or reduction)	USPAT; US-PGPUB	2001/11/04 15:50
19	5131	power with usage	USPAT; US-PGPUB	2001/11/04 15:50
22	587	((power with (save or saving or conserve or conserving or conservation or reduce or reducing or reduction)) or (power with usage)) same ((data with type))	USPAT; US-PGPUB	2001/11/04 15:51
25	8	(power same table) same (((power with (save or saving or conserve or conserving or conservation or reduce or reducing or reduction)) or (power with usage)) same ((data with type)))	USPAT; US-PGPUB	2001/11/04 15:54
28	8901	713/\$.ccls.	USPAT; US-PGPUB	2001/11/04 15:54
31	48	713/\$.ccls. and (((power with (save or saving or conserve or conserving or conservation or reduce or reducing or reduction)) or (power with usage)) same ((data with type)))	USPAT; US-PGPUB	2001/11/04 15:55

US-CL-CURRENT: 375/233,375/377 ,709/223

US-PAT-NO: 6092122

DOCUMENT-IDENTIFIER: US 6092122 A

TITLE: xDSL DMT modem using sub-channel selection to achieve scaleable data rate based on available signal processing resources

DATE-ISSUED: July 18, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Liu; Young Way	La Mirada	CA	N/A	N/A
Liu; Ming-Kang	Cupertino	CA	N/A	N/A
Chen; Steve	San Jose	CA	N/A	N/A

US-CL-CURRENT: 709/227,375/233 ,375/377 ,709/223

ABSTRACT:

A high speed modem is provided which uses a selectable, desirable portion of the total available bandwidth of a transmission channel. In a preferred embodiment, the invention is incorporated in a dedicated hardware circuit which

is connected on one end to a data processor and on the other end to an upstream

transceiver through a channel supporting an Asymmetric Digital Subscriber Loop (ADSL) standard. The achievable target data rate of the modem is based on the capabilities of an analog front end (AFE) used in the modem, and a signal processor within the dedicated hardware. In particular, the modem AFE contains

subband filtering which causes an upstream transceiver to use only a selected number of available sub-channels for downstream data transmission. The data rate of the modem is increased by upgrading the AFE or the signal processor in order to increase the number of processable transmitted downstream sub-channels.

70 Claims, 13 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 9

DEPR:

A calibration routine 520 is then executed to determine the nominal setup parameters for the overall system in the manner described earlier. The results

from this operation are stored in Device Parameter Table 560 where they then become accessible to various application programs that may make use of ADSL Modem Card 396 and Device Driver 400. The information stored in table 560 can include any or all of the following: (a) measurements of the computing power available to the host processor; (b) measurements of the number of frames processable by the system within a particular time period; (c) estimations of the expected loading on the processing system based on demands of other applications programs and peripheral devices; (d) minimum and maximum data throughput estimations and/or targets; (e) data identifying the type of host processor; (f) data identifying the number and type of AFEs in ADSL Modem card 396; (g) estimations and/or target system loading rates available for a datalink (i.e., maximum available processing time to be used by the system during data transmission); (h) data transmit and receive buffer sizes; (i) interrupt or similar priority data for the modem card; (j) estimations and/or target system sub-channel utilization; (k) estimations and/or target system sub-channel bit capacity information; etc. It will be apparent to skilled artisans that the above are just examples of the types of information that may

be pertinent to the performance of a high speed communications system, and that other parameters may be considered depending on the environment, application, etc. in which the present invention is used.

US-CL-CURRENT: 370/341

US-PAT-NO: 6065060

DOCUMENT-IDENTIFIER: US 6065060 A

TITLE: Modular multiplicative data rate modem and method of operation

DATE-ISSUED: May 16, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Liu; Young Way	La Mirada	CA	N/A	N/A
Liu; Ming-Kang	Cupertino	CA	N/A	N/A
Chen; Steve	San Jose	CA	N/A	N/A

US-CL-CURRENT: 709/233,370/341

ABSTRACT:

A high speed modem is provided which targets the use of a selectable, desirable portion of the total available bandwidth of a channel for achieving a data rate which nevertheless far exceeds that of conventional voice-band modems. In a preferred embodiment, the invention is implemented in an Asymmetric Digital Subscriber Loop (ADSL), and the nominal data rate is achieved using an analog front end (AFE) with subband filtering which causes an upstream transceiver to use only a selected number of available sub-channels for downstream data transmission and allows slower sampling rate for the AFE. The data rate of the modem is increased in a multiplicative fashion through modular expansion of a bank of AFEs to increase the number of transmitted downstream sub-channels.

38 Claims, 13 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 10

DEPR:

A calibration routine 520 is then executed to determine the nominal setup parameters for the overall system in the manner described earlier. The results from this operation are stored in Device Parameter Table 560 where they then become accessible to various application programs that may make use of ADSL Modem Card 396 and Device Driver 400. The information stored in table 560 can include any or all of the following: (a) measurements of the computing power available to the host processor, (b) measurements of the number of frames processable by the system within a particular time period; (c) estimations of the expected loading on the processing system based on demands of other applications programs and peripheral devices; (d) minimum and maximum data throughput estimations and/or targets; (e) data identifying the type of host processor, (f) data identifying the number and type of AFEs in ADSL Modem card 396; (g) estimations and/or target system loading rates available for a datalink (i.e., maximum available processing time to be used by the system during data transmission); (h) data transmit and receive buffer sizes; (i) interrupt or similar priority data for the modem card; (j) estimations and/or target system sub-channel utilization; (k) estimations and/or target system sub-channel bit capacity information; etc. It will be apparent to skilled artisans that the above are just examples of the types of information that may be pertinent to the performance of a high speed communications system, and that other parameters may be considered depending on the environment, application, etc. in which the present invention is used.

US-CL-CURRENT: 702/183,73/117.2

US-PAT-NO: 5038289

DOCUMENT-IDENTIFIER: US 5038289 A

TITLE: Diagnosis system for a motor vehicle

DATE-ISSUED: August 6, 1991

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Abe; Kunihiro	Higashimurayama	N/A	N/A	JPX

US-CL-CURRENT: 701/99,702/183 ,73/117.2

ABSTRACT:

A diagnosis system for diagnosing an electronic control system mounted on a vehicle has a signal transmitter for transmitting a data demand signal and a signal demanding termination of transmission of the data. The electronic control system has a signal receiver for receiving the data demand signal and the transmission terminating demand signal from the diagnosis device, and an interpreter for interpreting the content of the received signals and a signal transmitter for transmitting an output signal to the diagnosis device in accordance with the interpretation.

2 Claims, 13 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 13

DEPR:

Referring to FIGS. 6a to 6c, the electronic control system 101, 102, 103 and 104 have central processor units (CPUs) 1a, 2a, 3a and 4a, random access memories (RAMs) 1b, 2b, 3b and 4b, read only memories (ROMs) 1c, 2c, 3c and 4c, non-volatile random access memories (non-volatile RAMs) 1d, 2d, 3d and 4d, input interfaces 1g, 2g, 3g and 4g, and output interfaces 1e, 2e, 3e and 4e, respectively. The CPU, RAMs, ROM, input and output interfaces in each control system are connected to each other through a bus line. In the RAMs 1b to 4b, various processed parameters and tables are stored. Programs and data for controlling the engine and fixed data such as the type of the vehicle are stored in the ROMs 1c to 4c. Power is supplied to the CPUs, input and output interfaces, and drivers of control systems from the source BV.

US-CL-CURRENT: 370/252

US-PAT-NO: 6075770

DOCUMENT-IDENTIFIER: US 6075770 A

TITLE: Power spectrum-based connection admission control for ATM networks

DATE-ISSUED: June 13, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chang; Chung-Ju	Taipei	N/A	N/A	TWX
Chi; Hung-Ming	Taichung	N/A	N/A	TWX
Cheng; Ray-Guang	Keelung	N/A	N/A	TWX
Lin; Tzung-Pao	Kaohsiung	N/A	N/A	TWX
Wang; Yao-Tzung	Hsinchu	N/A	N/A	TWX

US-CL-CURRENT: 370/395.21, 370/252

ABSTRACT:

A method and system are disclosed for constructing a power spectrum based connection admission control table and using such a table in a communications network, such as an ATM network. Power spectrum parameters, such as the power spectrum DC component γ , half power bandwidth $B_{sub.w}$ and average power $PSI_{sub.w}$ are transformed to γ , an equivalent half power bandwidth $B_{sub.e}$ and an equivalent average power $PSI_{sub.e}$, where $B_{sub.e}$ is a predetermined constant. Since $B_{sub.e}$ is constant, the transformation reduces the memory requirements for constructing a connection admission control table. 22 Claims, 16 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 7

DEPR:

Note that the illustration herein assumes that transactional data communications are to be accommodated in addition to streamed data communications. If only streamed data communications are to be accommodated, the power spectrum based admissions control table may be generated by storing values of $PSI_{sub.max}$ ($\gamma_{sub.T}$) that depend only on the type-1 traffic load parameter $\gamma_{sub.T}$. In any event, note the dramatic reduction in the

size of the power spectrum based admission control table 114 that results by the conversion of parameters (γ , $B_{sub.w}$, and $PSI_{sub.w}$) to (γ , $B_{sub.e}$, and $PSI_{sub.e}$). In particular, because $B_{sub.e}$ is constant for each

call set up request, $PSI_{sub.max}$ is a function of only γ and not both γ and $B_{sub.e}$. Stated another way, $PSI_{sub.max}$ only varies for differing values of γ as there is only one possible value of $B_{sub.e}$ for

each call setup request. Thus, table entries need only be provided for each value of one parameter, namely, γ and not one for each possible pair of two varying parameters both γ and $B_{sub.e}$.

US-CL-CURRENT: 372/26,372/29.014

US-PAT-NO: 5917637

DOCUMENT-IDENTIFIER: US 5917637 A

TITLE: Method of and device for driving optical modulator, and optical communications system

DATE-ISSUED: June 29, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ishikawa; George	Kawasaki	N/A	N/A	JPX
Nishimoto; Hiroshi	Kawasaki	N/A	N/A	JPX

US-CL-CURRENT: 359/181,372/26 ,372/29.014

ABSTRACT:

A device and a method for driving an electro-absorption optical modulator for receiving carrier light emitted from a light source and outputting signal light subjected to intensity modulation according to the absorption of the carrier light. A bias circuit generates a bias voltage determined so that the optical modulator has a given chirping parameter. A driving circuit generates a modulating signal corresponding to an input signal, superimposes the modulating signal on the bias voltage, and supplies the superimposed signal to the optical modulator. A control circuit controls at least one parameter selected from a parameter group including the amplitude and duty of the modulating signal and the power of the carrier light, based on the bias voltage. It can be possible to provide a method of and a device for driving an

optical modulator capable of arbitrarily setting a chirping parameter.

29 Claims, 16 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 12

DEPR:

When the temperature of MI-LD 12 is raised in the optical transmitter shown in FIG. 10, the degree or level of wavelength detuning between the LD 16 and the EA modulator 20, i.e., the difference between the wavelength of the carrier light outputted from the LD 16 and a wavelength which provides a band gap in the EA modulator 20 is reduced so that the extinction ratio is improved. This reduction can be understood from a variation in the shape of a characteristic curve which relates the power of the output light to the applied voltage. Thus, since the optimum values of other drive parameters to be controlled vary due to a change in characteristic curve when the temperature is of an object to

be controlled, it is desired that the ROM 42 includes a data table set in advance for each value of temperature. In the given embodiment of the present invention as described above, the control means 10 shown in FIG. 1 includes a means for controlling the temperature of the EA modulator in such a manner that

the temperature rises as the bias voltage applied to the EA modulator 4 increases. It should be also considered that when this type of data table is created, the power of the carrier light is reduced as the temperature of the LD 16 rises.

US-CL-CURRENT: 326/53,326/95 ,327/294 ,327/3 ,368/201 ,968/905 ,968/920 ,968/DIG.1

US-PAT-NO: 4024416

DOCUMENT-IDENTIFIER: US 4024416 A

TITLE: Method for controlling frequency of electrical oscillations and frequency standard for electronic timepiece

DATE-ISSUED: May 17, 1977

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Fujita; Hiro	Sayama	N/A	N/A	JA
Morokawa; Shigeru	Higashiyamato	N/A	N/A	JA
Tsuzuki; Akira	Tokyo	N/A	N/A	JA

US-CL-CURRENT: 327/115,326/53 ,326/95 ,327/294 ,327/3 ,368/201 ,968/905 ,968/920 ,968/DIG.1

ABSTRACT:

A frequency standard for an electronic timepiece comprising a low frequency oscillator and a high frequency oscillator of which the frequency is an integral multiple of a predetermined frequency of the lower frequency oscillator. A phase difference detector is coupled to the lower and higher frequency oscillators to produce a signal occurring at intervals depending on the phase difference between the two oscillators. A frequency divider is provided to divide down the frequency of the signal by the integral multiple to

produce a phase difference signal. The phase difference signal is algebraically added to the lower frequency oscillator signal to generate an output signal of which frequency is equal to that of the high or frequency oscillation signal divided by the integral multiple.

22 Claims, 17 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 13

DEPR:

A second embodiment of the present invention is illustrated in FIG. 5 and will be explained with reference to FIG. 6 and Tables 1 and 2. The circuit shown in

FIG. 5 comprises a high frequency signal source 11 and a low frequency signal source 12. The sources 11 and 12 generate signals at the same frequencies as in the previous embodiment, but the signal at the lower frequency has a pulse duty cycle of considerably less than 50%, to reduce time intervals in which the

higher frequency signal passes through the flip-flop 40 to thereby minimize power requirement. The signal at the higher frequency is applied to the data input terminal of a data-type edge-triggered flip-flop 40. Flip-flop 40 comprises a data channel 41 which includes transmission gates 42 and 43, a first pair of unity-gain inverting amplifiers 44, 45 connected between the output and input of gates 42 and 43 respectively, and a second pair of unity-gain inverting amplifiers 46, 47 connected between the output of gate 43 and the Q output terminal of the flip-flop 40. A first feedback transmission gate 48 is coupled in parallel with the first inverter pair 44, 45 to provide a

first feedback memory path, and a second feedback transmission gate 49 is coupled in parallel with the second inverter pair 46, 47 to provide a second feedback memory path. The signal at the lower frequency is applied directly to

the control terminals of gates 42 and 49, and through inverters 50 and 51 to

the control terminals of gates 43 and 48, respectively. The connection between low frequency signal source 12 and flip-flop 40 serves to trigger this flip-flop and the corresponding terminal is therefore termed the trigger or clock input terminal of the flip-flop.

US-CL-CURRENT: 713/323

US-PAT-NO: 6282667

DOCUMENT-IDENTIFIER: US 6282667 B1

TITLE: Method and apparatus for selectively powering circuitry within a sound device to perform selected sound functions

DATE-ISSUED: August 28, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nakazato; Ryu	Yokohama	N/A	N/A	JPX

US-CL-CURRENT: 713/324, 713/323

ABSTRACT:

A sound controller comprises circuitry that performs a variety of sound functions. The circuitry is only powered when required by an application program. A power-saving driver receives a message issued from an operating system. When the message means indicates that a sound function is starting to be used, the power-saving driver turns on the power supply of a sound controller and then hands over the message to the sound device driver. In contrast, when the message indicates that the use of the sound function is ending, the power-saving driver first hands over the message to the sound driver, thereby causing the sound driver to execute an end process. After a predetermined time has elapsed since the power-saving driver handed over the message, it turns off the power supply of the sound controller.

4 Claims, 10 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 7

DEPR:

When receiving, for example, an open message to start the execution of the WAVE-type sound function from the power-saving driver 34, the sound device driver 33 drives and controls the sound controller 18 to cause the WAVE-type sound data sent via an expansion bus to be subjected to a sound process..

DEPR:

When receiving a close message to end the execution of the WAVE-type sound function from the power-saving driver 34, the sound device driver 33 controls the sound controller 18 to stop the processing of the WAVE-type sound data.

CCOR:

713/324

CCXR:

713/323

US-CL-CURRENT: 713/323

US-PAT-NO: 6282667

DOCUMENT-IDENTIFIER: US 6282667 B1

TITLE: Method and apparatus for selectively powering circuitry within a sound device to perform selected sound functions

DATE-ISSUED: August 28, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nakazato; Ryu	Yokohama	N/A	N/A	JPX

US-CL-CURRENT: 713/324, 713/323

ABSTRACT:

A sound controller comprises circuitry that performs a variety of sound functions. The circuitry is only powered when required by an application program. A power-saving driver receives a message issued from an operating system. When the message means indicates that a sound function is starting to be used, the power-saving driver turns on the power supply of a sound controller and then hands over the message to the sound device driver. In contrast, when the message indicates that the use of the sound function is ending, the power-saving driver first hands over the message to the sound driver, thereby causing the sound driver to execute an end process. After a predetermined time has elapsed since the power-saving driver handed over the message, it turns off the power supply of the sound controller.

4 Claims, 10 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 7

DEPR:

When receiving, for example, an open message to start the execution of the WAVE-type sound function from the power-saving driver 34, the sound device driver 33 drives and controls the sound controller 18 to cause the WAVE-type sound data sent via an expansion bus to be subjected to a sound process..

DEPR:

When receiving a close message to end the execution of the WAVE-type sound function from the power-saving driver 34, the sound device driver 33 controls the sound controller 18 to stop the processing of the WAVE-type sound data.

CCOR:

713/324

CCXR:

713/323

US-CL-CURRENT: 713/600

US-PAT-NO: 6079024

DOCUMENT-IDENTIFIER: US 6079024 A

TITLE: Bus interface unit having selectively enabled buffers

DATE-ISSUED: June 20, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hadjimohammadi; Massoud	Morgan Hill	CA	N/A	N/A
Asthana; Sunil K.	Freemont	CA	N/A	N/A

US-CL-CURRENT: 713/322, 713/600

ABSTRACT:

A computer system includes a bus interface with a plurality of data buffers.

Each data buffer is clocked by an individual clock signal. To reduce the power

consumption of the bus interface unit, the clock signals of the data buffers that are inactive are disabled during the period of inactivity. The bus interface unit includes a clock control unit that monitors a data bus coupled to the bus interface to determine when a bus cycle begins and the type of bus cycle. The clock control unit additionally monitors memory and CPU buffer signals that indicate which, if any, buffers are being accessed by the memory or CPU. From this information, the clock control unit determines which buffers

are active and inactive, and outputs control signals to a clock unit to disable

the clock signals associated with inactive buffers.

23 Claims, 5 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 5

ABPL:

A computer system includes a bus interface with a plurality of data buffers.

Each data buffer is clocked by an individual clock signal. To reduce the power

consumption of the bus interface unit, the clock signals of the data buffers that are inactive are disabled during the period of inactivity. The bus interface unit includes a clock control unit that monitors a data bus coupled to the bus interface to determine when a bus cycle begins and the type of bus cycle. The clock control unit additionally monitors memory and CPU buffer signals that indicate which, if any, buffers are being accessed by the memory or CPU. From this information, the clock control unit determines which buffers

are active and inactive, and outputs control signals to a clock unit to disable

the clock signals associated with inactive buffers.

BSPR:

The present invention still further contemplates a method of reducing power dissipation in a bus interface unit coupled to a data transfer bus including: enabling clock signals to a plurality of transmit and receive buffers at the beginning of a bus cycle of the data transfer bus; decoding control signals of the data transfer bus to determine a cycle type of the bus cycle; determining which of the plurality transmit and receive buffers are inactive during the bus

cycle; and disabling clocks signals to the transmit and receive buffers that are inactive during the bus cycle.

CCOR:

713/322

CCXR:

713/600

US-CL-CURRENT: 709/103,713/324

US-PAT-NO: 6065123

DOCUMENT-IDENTIFIER: US 6065123 A

TITLE: Computer system with unattended on-demand availability

DATE-ISSUED: May 16, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chou; Stephen T.	Beaverton	OR	N/A	N/A
Fenger; Russell J.	Aloha	OR	N/A	N/A
Kumar; Mohan J.	Beaverton	OR	N/A	N/A
Lortz; Victor B.	Beaverton	OR	N/A	N/A
Manny; Benjamin L.	Portland	OR	N/A	N/A
Travnicek; Mil	Portland	OR	N/A	N/A
Wang; Chih-Kan	Portland	OR	N/A	N/A

US-CL-CURRENT: 713/322, 709/103 , 713/324

ABSTRACT:

A computer system with unattended on-demand availability includes power-saving features which place the system into a Standby mode whenever the system is idle or is not being used. Prior to entering Standby mode, the system sets a hardware timer which indicates when the next scheduled event in the system should be performed. When either the timer expires or another event

occurs which requires system operation, the system resumes to the On power state without user intervention. In one embodiment, the system of the present invention allows applications to periodically save their operational states. By saving their operational states, applications are able to guard against power failures and crashes. If a power failure or crash occurs, the system consults restart policies and, if appropriate, automatically re-starts applications to their most recently saved operational states once power is re-stored.

20 Claims, 17 Drawing figures

Exemplary Claim Number: 8

Number of Drawing Sheets: 10

DEPR:

Message field 650 indicates the type of message and any data associated with that message. In one implementation, the message type can be no message, a conventional Windows.TM. message, a user-defined message, a save checkpoint message, a request for the application to exit, an about to enter Standby

power

mode message, and a just entered normal power mode message. In one implementation, if a message is scheduled to be sent to an application which is

not connected to InstantON servicing agent 140, then InstantON servicing agent 140 queues the message for a period of time and delivers the message to the target if it connects before the application process exits. If the target application does not connect before it exits, then the message is deleted.

CCOR:

713/322

CCXR:

713/324

US-CL-CURRENT: 705/26, 713/167

US-PAT-NO: 5982891

DOCUMENT-IDENTIFIER: US 5982891 A

TITLE: Systems and methods for secure transaction management and electronic rights protection

DATE-ISSUED: November 9, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ginter; Karl L.	Beltsville	MD	N/A	N/A
Shear; Victor H.	Bethesda	MD	N/A	N/A
Spahn; Francis J.	El Cerrito	CA	N/A	N/A
Van Wie; David M.	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 705/54, 705/26, 713/167

ABSTRACT:

The present invention provides systems and methods for secure transaction management and electronic rights protection. Electronic appliances such as computers equipped in accordance with the present invention help to ensure that information is accessed and used only in authorized ways, and maintain the integrity, availability, and/or confidentiality of the information. Such electronic appliances provide a distributed virtual distribution environment (VDE) that may enforce a secure chain of handling and control, for example, to control and/or meter or otherwise monitor use of electronically stored or disseminated information. Such a virtual distribution environment may be used to protect rights of various participants in electronic commerce and other electronic or electronic-facilitated transactions. Distributed and other operating systems, environments and architectures, such as, for example, those using tamper-resistant hardware-based processors, may establish security at each node. These techniques may be used to support an all-electronic information distribution, for example, utilizing the "electronic highway."

102 Claims, 153 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 146

BSPV:

employ "templates" to ease the process of configuring capabilities of the present invention as they relate to specific industries or businesses. Templates are applications or application add-ons under the present invention. Templates support the efficient specification and/or manipulation of criteria related to specific content types, distribution approaches, pricing mechanisms,

user interactions with content and/or administrative activities, and/or the like. Given the very large range of capabilities and configurations supported by the present invention, reducing the range of configuration opportunities to a manageable subset particularly appropriate for a given business model allows the full configurable power of the present invention to be easily employed by "typical" users who would be otherwise burdened with complex programming and/or

configuration design responsibilities template applications can also help ensure that VDE related processes are secure and optimally bug free by reducing

the risks associated with the contribution of independently developed load modules, including unpredictable aspects of code interaction between independent modules and applications, as well as security risks associated with

possible presence of viruses in such modules. VDE, through the use of templates, reduces typical user configuration responsibilities to an appropriately focused set of activities including selection of method types (e.g. functionality) through menu choices such as multiple choice, icon selection, and/or prompting for method parameter data (such as identification information, prices, budget limits, dates, periods of time, access rights to specific content, etc.) that supply appropriate and/or necessary data for control information purposes. By limiting the typical (non-programming) user to a limited subset of configuration activities whose general configuration environment (template) has been preset to reflect general requirements corresponding to that user, or a content or other business model can very substantially limit difficulties associated with content containerization (including placing initial control information on content), distribution, client administration, electronic agreement implementation, end-user interaction, and clearinghouse activities, including associated interoperability problems (such as conflicts resulting from security, operating system, and/or certification incompatibilities). Use of appropriate VDE templates can assure users that their activities related to content VDE containerization, contribution of other control information, communications, encryption techniques and/or keys, etc. will be in compliance with specifications for their distributed VDE arrangement. VDE templates constitute preset configurations that can normally be reconfigurable to allow for new and/or modified templates that reflect adaptation into new industries as they evolve or to reflect the evolution or other change of an existing industry. For example, the template concept may be used to provide individual, overall frameworks for organizations and individuals that create, modify, market, distribute, consume, and/or otherwise use movies, audio recordings and live performances, magazines, telephony based retail sales, catalogs, computer software, information data bases, multimedia, commercial communications, advertisements, market surveys, infomercials, games, CAD/CAM services for numerically controlled machines, and the like. As the context surrounding these templates changes or evolves, template applications provided under the present invention may be modified to meet these changes for broad use, or for more focused activities. A given VDE participant may have a plurality of templates available for different tasks. A party that places content in its initial VDE container may have a variety of different, configurable templates depending on the type of content and/or business model related to the content. An end-user may have different configurable templates that can be applied to different document types (e-mail, secure internal documents, database records, etc.) and/or subsets of users (applying differing general sets of control information to different bodies of users, for example, selecting a list of users who may, under certain preset criteria, use a certain document). Of course, templates may, under certain circumstances have fixed control information and not provide for user selections or parameter data entry.

CCXR:

713/167

US-CL-CURRENT: 713/340, 714/15

US-PAT-NO: 5978922

DOCUMENT-IDENTIFIER: US 5978922 A

TITLE: Computer system having resume function

DATE-ISSUED: November 2, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Arai; Makoto	Tokyo	N/A	N/A	JPX
Sato; Shigenobu	Iruma	N/A	N/A	JPX
Muraya; Hideaki	Tokyo	N/A	N/A	JPX
Kato; Keiichi	Tokyo	N/A	N/A	JPX
Tsukada; Hiroyuki	Tokyo	N/A	N/A	JPX

US-CL-CURRENT: 713/323, 713/340 , 714/15

ABSTRACT:

A computer system having a hibernation-type resume function which is performed by using an HDD. Provided on the hard disk of the HDD are storage area for storing ordinary data. Also provided on the hard disk is a resume storage area which is large enough to save resume data required to perform a resume operation. The resume storage area is controlled by a BIOS provided for

performing the resume operation, not by the operating system (OS) of the computer system. The BIOS accesses the resume storage area when the power supply to the system is switched off, thereby saving the resume data in a resume data memory.

40 Claims, 15 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 12

BSPR:

Battery-driven, portable personal computers have resume function. When a personal computer of this type is switched off, or more precisely when its power switch is turned off, the data items representing the conditions the display panel, the computer and the application program assume immediately before the power switch is turned off are saved in a memory which is driven by the battery. When the power switch is turned on, the display panel, the computer and the application program resumes the conditions represented by the data items saved in the battery-driven memory. Thus, the personal computer can

be operated again in exactly the same conditions it assumed when the power switch was turned off. Saving these data items in the memory when the computer

is turned off is known as "suspend operation." Thanks to the resume function, the information and the status data respectively stored in the main memory and the CPU internal register can be saved when the power switch is turned off and can be restored when the power switch is turned on.

BSPR:

Fourth, hibernation-type resume operation consumes far more power than normal-type resume operation. This is because much power is required to drive the HDD in the hibernation-type resume operation, whereas a small amount of power is sufficient to save the data items in a battery-driven memory in the normal-type resume operation. The battery loaded in a portable personal computer has but a small capacity. The amount of power it accumulates by a single recharging is much limited. The power remaining in the battery may not be sufficient to drive the HDD when the computer is turned off. In this case,

the data items which the computer needs to resume its last operating conditions cannot be saved in the HDD. In other words, the hibernation-type resume function cannot work at all.

CCOR:

713/323

CCXR:

713/340

US-CL-CURRENT: 345/555,711/100 ,713/320

US-PAT-NO: 5961617

DOCUMENT-IDENTIFIER: US 5961617 A

TITLE: System and technique for reducing power consumed by a data transfer operations during periods of update inactivity

DATE-ISSUED: October 5, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tsang; Siu Keun	Saratoga	CA	N/A	N/A

US-CL-CURRENT: 710/100,345/555 ,711/100 ,713/320

ABSTRACT:

A system and method are described that reduce display subsystem power consumption in computer systems where image data is transferred from an image memory to a display each time a new image frame is displayed. In normal operation, the computer system displays uncompressed image data, which is stored in the image memory. After a period of display inactivity, a display processor compresses the uncompressed data and writes the compressed data to another location in the image memory. In subsequent display cycles, until there is display activity, the display processor retrieves the compressed data from the memory, decompresses it in real time and then transfers the decompressed data to the display. Entire images or segments of images can be compressed in this manner. Using the compressed image data saves display power

as it requires fewer memory cycles to transfer from the memory to the display than the uncompressed data. Bus bandwidth available for other, unrelated activities increases as the result of this bandwidth reduction, which benefits other system operations.

31 Claims, 7 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 7

BSPR:

The processing unit, memory and bus can be deployed within a computer system with limited power reserves (e.g., a handheld, portable or battery-powered system). In such a system the power savings provided by the present invention would substantially increase battery life and/or system performance. In any of

the embodiments, the input data can be display data, in which case the processing unit performs graphical display operations and the output data is graphics data. The input data can also be any other type of data associated with repetitive and continuous data operations.

CCXR:

713/320

US-CL-CURRENT: 713/324

US-PAT-NO: 5845291

DOCUMENT-IDENTIFIER: US 5845291 A

TITLE: Computer with reduced power consumption

DATE-ISSUED: December 1, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Winokur; Alex	Haifa	N/A	N/A	ILX

US-CL-CURRENT: 707/200, 713/324

ABSTRACT:

A computer is disclosed having a semiconductor memory; a disk data storage device of the type which automatically switches to a low power consumption mode when disk access is not required; and means for associating an application program with a plurality of data files which are usable by the application. The computer is arranged to load the plurality of data files from the disk data storage device into the semiconductor memory before use of the application and to save at least any modified ones of the plurality of files back to the disk data storage device after use of the application. In this way, access to the disk data storage device is not required during use of the application program, thereby reducing power consumption of the device.

8 Claims, 3 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 2

ABPL:

A computer is disclosed having a semiconductor memory; a disk data storage device of the type which automatically switches to a low power consumption mode when disk access is not required; and means for associating an application program with a plurality of data files which are usable by the application. The computer is arranged to load the plurality of data files from the disk data storage device into the semiconductor memory before use of the application and to save at least any modified ones of the plurality of files back to the disk data storage device after use of the application. In this way, access to the disk data storage device is not required during use of the application program, thereby reducing power consumption of the device.

BSPR:

This invention is directed to the problem of reducing the power consumption of computers comprising a disk data storage device of the above described type.

BSPR:

This invention provides a computer having a semiconductor memory; a disk data storage device of the type which automatically switches to a low power consumption mode when disk access is not required; and means for associating an application program with a plurality of data files which are usable by the application, characterised in that the computer is arranged to load the plurality of data files from the disk data storage device into the

semiconductor memory before use of the application and to save at least any modified ones of the plurality of files back to the disk data storage device after use of the application so that access to the disk data storage device is not required during use of the application program.

BSPR:

Viewed from another aspect there is provided a method of executing an application program in a computer having a semiconductor memory; a disk data storage device of the type which automatically switches to a low power consumption mode when disk access is not required; and means for associating an application program with a plurality of data files which are usable by the application, comprising the steps of loading the plurality of data files from the disk data storage device into the semiconductor memory before use of the application and saving at least any modified ones of the plurality of files back to the disk data storage device after use of the application so that access to the disk data storage device is not required during use of the application program.

CCXR:

713/324

US-CL-CURRENT: 713/1, 714/15

US-PAT-NO: 5832283

DOCUMENT-IDENTIFIER: US 5832283 A

TITLE: Method and apparatus for providing unattended on-demand availability of
a computer system

DATE-ISSUED: November 3, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chou; Stephen T.	Beaverton	OR	N/A	N/A
Fenger; Russell J.	Aloha	OR	N/A	N/A
Kumar; Mohan J.	Beaverton	OR	N/A	N/A
Lortz; Victor B.	Beaverton	OR	N/A	N/A
Manny; Benjamin L.	Portland	OR	N/A	N/A
Travnicek; Mil	Portland	OR	N/A	N/A
Wang; Chih-Kan	Portland	OR	N/A	N/A

US-CL-CURRENT: 713/300, 713/1 , 714/15

ABSTRACT:

A computer system with unattended on-demand availability includes power-saving features which place the system into a Standby mode whenever the system is idle or is not being used. Prior to entering Standby mode, the system sets a hardware timer which indicates when the next scheduled event in the system should be performed. When either the timer expires or another event

occurs which requires system operation, the system resumes to the On power state without user intervention. In one embodiment, the system of the present invention allows applications to periodically save their operational states. By saving their operational states, applications are able to guard against power failures and crashes. If a power failure or crash occurs, the system consults restart policies and, if appropriate, automatically re-starts applications to their most recently saved operational states once power is re-stored.

20 Claims, 17 Drawing figures

Exemplary Claim Number: 17

Number of Drawing Sheets: 10

DEPR:

Message field 650 indicates the type of message and any data associated with that message. In one implementation, the message type can be no message, a conventional Windows.TM. message, a user-defined message, a save checkpoint message, a request for the application to exit, an about to enter Standby

power

mode message, and a just entered normal power mode message. In one implementation, if a message is scheduled to be sent to an application which is

not connected to InstantON servicing agent 140, then InstantON servicing agent 140 queues the message for a period of time and delivers the message to the target if it connects before the application process exits. If the target application does not connect before it exits, then the message is deleted.

CCOR:

713/300

CCXR:

713/1

US-CL-CURRENT: 713/100, 713/320

US-PAT-NO: 5754798

DOCUMENT-IDENTIFIER: US 5754798 A

TITLE: Computer system with function for controlling system configuration and power supply status data

DATE-ISSUED: May 19, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Uehara; Keiichi	Tokyo	N/A	N/A	JPX
Inomata; Tadaaki	Tokyo	N/A	N/A	JPX

US-CL-CURRENT: 710/104, 713/100 , 713/320

ABSTRACT:

Since an instruction of switching of the system operation environment or configuration such as the power save mode and power-up mode is input by the hot

key operation using SMI, key data of the hot key can be instantly received by the CPU even while any type of application program is being executed, and the operation environment is changed. Further, when the system operation environment or configuration such as the power save mode and power-up mode is changed, a pop-up window indicating the present system operation environment is

automatically opened on the display image plane according to the rewritten operation environment or system configuration data of the CMOS memory.

Therefore, the operation mode switched by the hot key function can be instantly

indicated to the user. When an event mode is set, in response to a change of a

power supply status, a power supply controller set data indicating the changing

of the power supply status, into a predetermined register of the computer system. At this time, the power supply controller informs the CPU of the changing of the power supply status by using an interrupt signal.

24 Claims, 15 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 13

ABPL:

Since an instruction of switching of the system operation environment or configuration such as the power save mode and power-up mode is input by the hot

key operation using SMI, key data of the hot key can be instantly received by the CPU even while any type of application program is being executed, and the operation environment is changed. Further, when the system operation environment or configuration such as the power save mode and power-up mode is changed, a pop-up window indicating the present system operation environment is

automatically opened on the display image plane according to the rewritten operation environment or system configuration data of the CMOS memory.

Therefore, the operation mode switched by the hot key function can be instantly

indicated to the user. When an event mode is set, in response to a change of a

power supply status, a power supply controller set data indicating the changing

of the power supply status, into a predetermined register of the computer

system. At this time, the power supply controller informs the CPU of the changing of the power supply status by using an interrupt signal.

DEPR:

As described above, in this embodiment, since instruction of switching of the system operation environment or configuration such as the power save mode and power-up mode is input by the hot key operation using SMI, hot key data of the hot key can be instantly received by the CPU 11 even if any type of application program is being executed, and the operation environment is changed. Further, when the system operation environment or configuration such as the power save mode and power-up mode is changed, the pop-up window indicating the present system operation environment or configuration is automatically opened on the display image plane according to the rewritten operation environment or system configuration data of the CMOS memory 251. Therefore, even if a display lamp or display unit exclusively used for status display is not provided on the computer body as in the conventional system having the hot key function, the operation mode switched by the hot key function can be instantly indicated to the user.

CCXR:

713/100

CCXR:

713/320

US-CL-CURRENT: 700/286, 713/300 , 713/322 , 713/323 , 713/601

US-PAT-NO: 5737616

DOCUMENT-IDENTIFIER: US 5737616 A

TITLE: Power supply circuit with power saving capability

DATE-ISSUED: April 7, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Watanabe; Mitsuhiro	Tokyo	N/A	N/A	JPX

US-CL-CURRENT: 713/340, 700/286 , 713/300 , 713/322 , 713/323 , 713/601

ABSTRACT:

A power supply circuit efficiently saves electric energy consumed by a central processing unit and a peripheral assembly through coordination between power supply modes of the central processing unit and the peripheral assembly. The central processing unit has a register for establishing a status of an internal power supply of the central processing unit, a first mechanism for changing the internal power supply into the status established by the register,

and a second mechanism for outputting a status signal indicative of the status.

The peripheral assembly having a peripheral circuit, a peripheral device, and a

power supply control block for changing power supply statuses and clock statuses of the peripheral circuit and the peripheral device based on the status signal outputted from the second mechanism.

8 Claims, 11 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 10

DEPR:

FIG. 2 shows in block form the power supply circuit with the power saving capability according to the second embodiment of the present invention, the power supply circuit being incorporated in a system including a CPU, a peripheral assembly, and respective buses. The power supply circuit according to the second embodiment is used mainly in combination with CPUs such as DSP CPUs, CISC and RISC CPUs. The principles of the present invention are based on

the relationship between a power supply controller in a CPU and a power supply controller in a peripheral assembly, and does not depend on the type of buses for accessing data. Therefore, the power supply circuit according to the second embodiment is basically the same as the power supply circuit according to the first embodiment, and will not be described in detail below except its structural details.

DEPR:

FIG. 8 shows in block form the power supply circuit with the power saving capability according to the fourth embodiment of the present invention, the power supply circuit being incorporated in a system including a CPU, a peripheral assembly, and respective buses. The power supply circuit according to the fourth embodiment is used mainly in combination with CPUs such as DSP CPUs, CISC and RISC CPUs. The principles of the present invention are based on

the relationship between a power supply controller in a CPU and a power supply controller in a peripheral assembly, and does not depend on the type of buses for accessing data. Therefore, the power supply circuit according to the fourth embodiment is basically the same as the power supply circuit according

to the third embodiment, and will not be described in detail below except its structural details.

CCOR:

713/340

CCXR:

713/300

CCXR:

713/322

CCXR:

713/323

CCXR:

713/601

US-CL-CURRENT: 323/300,326/63 ,326/81 ,363/74 ,702/60 ,713/340

US-PAT-NO: 5734585

DOCUMENT-IDENTIFIER: US 5734585 A

TITLE: Method and apparatus for sequencing power delivery in mixed supply computer systems

DATE-ISSUED: March 31, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Beard; Paul	Milpitas	CA	N/A	N/A

US-CL-CURRENT: 700/286,323/300 ,326/63 ,326/81 ,363/74 ,702/60 ,713/340

ABSTRACT:

The present invention discloses a sequence and circuitry for powering a mixed logic voltage computer system wherein power is delivered to the system hardware in increasing order according to the power consumption level of the particular system hardware such that system power consumption during system startup is minimized.

3 Claims, 3 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 3

BSPR:

Computer systems are becoming increasingly more portable while at the same time

becoming increasingly more powerful. Low power consumption is an essential design criterion of portable battery powered computer systems and data terminals. For this reason much of the hardware in a portable computer system,

such as the system microprocessor, operates at lower logical voltage supply levels, typically 3.3 volts, because systems operating at lower voltages consume less power than systems operating at higher voltages. The most common computer hardware devices operate at 5.0 volts for logic voltage levels.

Portable data terminals and other laptop type computer systems employ microprocessors and other hardware devices which operate at 3.3 volts for logic

voltage levels in order to reduce system power consumption and thereby extend operational battery time.

CCXR:

713/340

US-CL-CURRENT: 710/15,710/17 ,710/18

US-PAT-NO: 5675814

DOCUMENT-IDENTIFIER: US 5675814 A

TITLE: Apparatus and method for managing power consumption by I/O ports in a computer system

DATE-ISSUED: October 7, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Pearce, John J.	Austin	TX	N/A	N/A

US-CL-CURRENT: 713/324,710/15 ,710/17 ,710/18

ABSTRACT:

A portable computer is provided in which the consumption of power by the I/O ports of the computer is reduced. The processor of the computer distinguishes port I/O operations that require an actual data transfer from port I/O operations that do not require an actual data transfer. The I/O ports of the computer remain off until an I/O operation involving an actual data transfer at a particular port is required. When an I/O operation which requires an actual data transfer is encountered, then the appropriate port is powered up. In this manner, power consumption by the I/O ports of the computer is significantly reduced. Advantageously, the disclosed technique for reducing power consumption by the I/O ports of the computer is operating system independent. In this manner, the power management feature functions regardless of which particular operating system or application software is installed on the computer.

33 Claims, 3 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 3

CLPV:

if the I/O type of the trapped I/O operation is that of an I/O activity without

data transfer through the I/O port, then emulating the trapped I/O operation, the I/O port remaining in a power conserving state during this emulating step;

CCOR:

713/324

US-CL-CURRENT: 713/300

US-PAT-NO: 5652893

DOCUMENT-IDENTIFIER: US 5652893 A

TITLE: Switching hub intelligent power management

DATE-ISSUED: July 29, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ben-Meir; Sam	Sharon	MA	N/A	N/A
Gibbons; John F.	Natick	MA	N/A	N/A
Thomas; Ian	Hopkinton	MA	N/A	N/A

US-CL-CURRENT: 713/310, 713/300

ABSTRACT:

A power management system rod for local area network hubs includes a network

switching hub with a connection backplane with a plurality of connection slots.

A power supply is provided having one or more elements providing a maximum power available for the system. Manageable modules are connected to said switching hub, each of said manageable modules having a memory providing information as to the power requirements of the module. A controller module is

connected to said manageable modules via said switching hub. The controller module includes memory means for receiving data from said manageable modules as

to power requirements. A microprocessor is provided for calculating power requirements of the system and for controlling the supply of power to each of said modules.

21 Claims, 4 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 4

DEPR:

It is noted that this configuration data is not saved locally on the DMM 30; it

is only maintained by the RCM 50 in the hub inventory. EEPROM 60. This information is needed by the RCM 50 after a hub is reset and before any modules

are power-enabled, hence, its placement in the hub inventory EEPROM 60.

Except

for slot type information, the data can be configured to meet specific hub power requirements. Whenever this intelligent power management configuration information is changed by either the RCM 50 or the DMM 30, the RCM 50 automatically saves the data in the hub inventory EEPROM 60; no action (like issuing the save command) is required on the EEPROM part of the DMM 30. By automatically saving this power management information, the data is consistent across hub resets, allowing the hub to return to its previous power states.

DEPR:

In general, whatever is stated about module 10, applies to module 30. Same issue for module 12 and module 8. Upon hub reset or power-up, the following conditions exist: all slots containing Modules 10 are power-disabled, and all slots containing modules 12 are power-enabled (because modules 12 are not power-manageable). The RCM 50 determines its initial power budget based on the

operational power supplies. The RCM 50 receives data as to the type and

capacity of each power supply 4 via input 92, connecting to the power supplies 4 over the backplane 2. RCM 50 also gathers inventory information from the hub inventory EEPROM 60, its own on-board inventory EEPROM 20, and the inventory EEPROM 20 for module and daughtercard. The inventory EEPROM for a module 10 or hub contains the module's/hub's power requirements in units of watts for each voltage line. The RCM 50 immediately reduces its power budget by the power requirements of 2 RCM 50s, regardless of whether there is actually a second RCM 50 in the hub, and the hub itself (e.g., the fan units draw power off +12 V). Since an RCM 50 is vital to hub operation and always consumes power (like a non-managed module), this method guarantees that the hot-insertion of a second RCM 50 does not impact hub operation in any way.

DEPR:

The RCM 50 also reads the saved power management configuration data from the hub inventory EEPROM 60. The RCM 50 verifies the data validity by comparing the saved slot profile against the current slot profile. This comparison is limited to verifying that for a given slot, the type of module (i.e., module 10, module 12, or empty) that is currently present in the slot matches the configuration data for the slot. If the slot profiles match, then the RCM 50 first reduces its power budget by the saved unmanaged power allocation. For each slot, it then restores the slot's power class and power state, if possible. Note that slots containing Modules 10 are power-enabled in order of power class (class 10 slots, then class 9 slots, and so on) based on the available power. It is possible that the RCM 50 will not be able to restore power to slots that were previously power-enabled if a power supply failed during the hub reset or power-cycle. After the slot power states are restored (as much as the power budget allows), the RCM 50 will restore the overheat automatic power-down mode and power fault-tolerant mode. In the case of power fault-tolerant mode, if it was previously enabled and sufficient power is available, then the RCM 50 will re-enter this mode; otherwise, until sufficient power is available, the hub will not operate in power fault-tolerant mode. By configuring power fault-tolerant mode last, the RCM 50 has power-enabled as many modules 10 as possible.

CCOR:

713/310

CCXR:

713/300

US-CL-CURRENT: 714/14,714/15

US-PAT-NO: 5339426

DOCUMENT-IDENTIFIER: US 5339426 A

TITLE: System and method for resume processing initialization

DATE-ISSUED: August 16, 1994

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Aoshima; Kinya	Fussa	N/A	N/A	JPX

US-CL-CURRENT: 713/1,714/14 ,714/15

ABSTRACT:

A resume processing driver for an advanced operating system, such as OS/2, is provided which saves data indicative of the operating conditions of the advanced operating system into system memory and then calls a previously existing resume processing routine designed for a previously existing operating system, such as MS-DOS. The previously existing resume processing routine performs additional processing in order to save operating condition data associated with the previously existing operating system into system memory, and then performs a controlled power off sequence and removes the power supplied to all elements of the computer except the computer memory. Thereafter, the existing resume processing routine performs processing to restore the operating condition data associated with the previously existing operating system from system memory and then passes control to the resume processing driver of the present invention. The resume processing driver restores the data indicative of the operating conditions of the advanced operating system from system memory, and control then passes to the computer program which was executing before the resume processing driver was initiated.

12 Claims, 11 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 10

DEPR:

Referring again to step 202, the resume processing driver of the present invention is executed after the NMI is detected by the CPU and the NMI is determined to be a result of the power-down switch being pressed. At this point, the resume driver performs various steps in order to properly save certain types of data associated with OS/2 into appropriate areas in the computer system's memory. After this is performed, the resume driver then transfers control to pre-existing ROM BIOS resume code which performs further resume processing functions and then physically removes power supplied to the various components of the computer system, except the memory. Thus, the resume

driver of the present invention, depicted in step 202, serves as a "wrapper" around the pre-existing ROM BIOS currently found in various computer systems, such as Toshiba laptops. That is, the resume driver saves the registers and data unique to the OS/2 operating system and/or the advanced microprocessor upon which OS/2 operates and places the computer system into a state in which the standard ROM BIOS resume processing routine is able to properly perform its

functionality and thereafter remove power from the various components.

CCOR:

713/1

US-CL-CURRENT: 708/111,708/136

US-PAT-NO: 5007015

DOCUMENT-IDENTIFIER: US 5007015 A

TITLE: Portable compact device

DATE-ISSUED: April 9, 1991

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yokozawa; Yukio	Nagano	N/A	N/A	JPX

US-CL-CURRENT: 713/1,708/111 ,708/136

ABSTRACT:

A portable compact device for use with an external device. The portable compact device includes an interface circuit for providing an interface between an external device and the portable compact device. A data memory circuit stores data received by the interface circuit. A control circuit coupled to the data memory circuit processes data stored in the data memory circuit in accordance with a stored data structure. A data modifying circuit is coupled to the data memory circuit for modifying the stored data. A data structure initializing circuit insures that the structure of the stored data in the data memory circuit allows the control circuit to process the stored data.

15 Claims, 9 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 6

BSPR:

Center controlling circuit 162 attempts to identify the type of data being input into the data input circuit 160 and, based on that information will properly process the data. In order to process the data at high speeds and with low electrical power usage, the structure of the input data is preset so as to include an indication of the type of data being transmitted. In addition, the data can be changed by way of a key input circuit 163.

CCOR:

713/1